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Substitute for form 1449A/PTO		Complete if Known			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/674,085		
		Filing Date	September 29, 2003		
		First Named Inventor	Elias Fallon et al.		
		Group Art Unit	Not Yet Assigned		
		Examiner Name	Not Yet Assigned		
Sheet	1	of	3	Attorney Docket Number	2879-030564

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ²			
	1	6,161,078		Ganley	12/12/2000	
	2	6,282,694		Cheng et al.	08/28/2001	
	3	6,550,046	B1	Balasa et al.	04/15/2003	

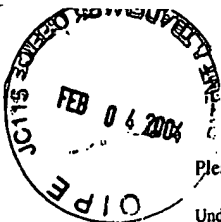
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HR	4	FLORIN BALASA and KOEN LAMPAERT, "Module Placement For Analog Layout Using The Sequence-Pair Representation", Proc. ACM/IEEE Design Automation, pp. 274-279, (June 1999).	
HR	5	FLORIN BALASA and KOEN LAMPAERT, "Symmetry Within The Sequence-Pair Representation In The Context Of Placement For Analog Design", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 19, No. 7, pp. 721-731 (July 2000).	
HR	6	FLORIN BALASA, "Device-Level Placement For Analog Layout: An Opportunity For Non-Slicing Topological Representations", Proc. Asia-Pacific DAC (ASPDAC), pp. 281-286, (2001).	
HR	7	ERIC FELT, ENRICO MALAVASI, EDOARDO CHARBON, ROBERTO TOTARO and ALBERTO SANGIOVANNI-VINCENTELLI, "Performance-Driven Compaction For Analog Integrated Circuits", IEEE 1993 Custom Integrated Circuits Conference, pp. 17.3.1-17.3.5, (1993).	
HR	8	ERIC FELT, EDOARDO CHARBON, ENRICO MALAVASI and ALBERTO SANGIOVANNI-VINCENTELLI, "An Efficient Methodology For Symbolic Compaction Of Analog IC's With Multiple Symmetry Constraints", Proc. European Design Automation Conference, pp. 148-153, (1992).	
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HR	10	PEI-NING GUO, CHUNG-KUAN CHENG and TAKESHI YOSHIMURA, "An O-Tree Representation Of Non-Slicing Floorplan And Its Applications", Proc. ACM/IEEE Design Automation Conference, pp. 268-273, (June 1999).	
HR	11	EN-CHENG LIU, MING-SHIUN LIN, JIANBANG LAI and TING-CHI WANG, "Slicing Floorplan Design With Boundary-Constrained Modules", ISPD'01, pp. 124-129, April 1-4 (2001).	
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Examiner Signature	<i>Steven Rosestete</i>	Date Considered	11/08/05
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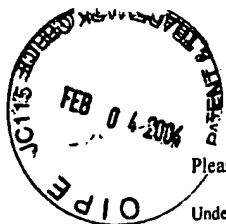
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HR	14	MARGHERITA PILLAN and DONATELLA SCIUTO, "Constraint Generation And Placement For Automatic Layout Design Of Analog Integrated Circuits", pp. 355-358.	
HR	15	YINGXIN PANG, FLORIN BALASA, KOEN LAMPAERT and CHUNG-KUAN CHENG, "Block Placement Symmetry Constraints Based On The O-Tree Non-Slicing Representation", Proc. ACM/IEEE Design Automation Conference, pp. 464-467, (June 2000).	
HR	16	JUAN A. PRIETO, JOSE M. QUINTANA, ADORACION RUEDA and JOSE L. HUERTAS, "An Algorithm For The Place-And-Route Problem In The Layout Of Analog Circuits", Pro. IEEE ISCAS, pp. 491-494 (1994).	
HR	17	D. F. WONG and C. L. LIU, "A New Algorithm For Floorplan Design", Proceedings Of The 23 rd ACM/IEEE Design Automation Conference, pp. 101-107, (July 1986).	
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	23	SUJOY MITRA, SUDIP K. NAG, ROB A. RUTENBAR and L. RICHARD CARLEY, "System-Level Routing Of Mixed-Signal ASICs In WREN", Proc. ACM/IEEE International Conference On CAD, pp. 394-399, (November 1992).	

Examiner Signature	<i>Robert Rosshesele</i>	Date Considered	11/08/05
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HR	24	R. OKUDA, T. SATO, H. ONODERA and K. TAMARU, "An Efficient Algorithm For Layout Compaction Problem With Symmetry Constraints", In Proc. IBBS ICCAD, pp. 148-151, (November 1989).	

Examiner Signature	<i>Helen Rosshebb</i>	Date Considered	11/08/08
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